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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte HARM PETER HOFSTEE, CHARLES RAY JOHNS, and
JAMES ALLAN KAHLE

Appeal 2009-010410[1]
Application 10/697,903
Technology Center 2100

Before JEAN R. HOMERE, JOHN A JEFFERY, and
DEBRA K. STEPHENS, *Administrative Patent Judges.*

HOMERE, *Administrative Patent Judge.*

DECISION ON APPEAL

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[1] The real party in interest is IBM Corp. (App. Br. 2.)

I. STATEMENT OF THE CASE

Appellants appeal under 35 U.S.C. § 134(a) from the final rejection of claims 8-27. Claims 1-7 have been canceled. (App. Br. 3.) We have jurisdiction under 35 U.S.C. § 6(b).

We reverse.

Appellants' Invention

Appellants invented a method and system for dynamically assigning interface pins in peripheral devices. In particular, upon receiving an assignment request for an interface pin, a flexible Input-Output (I/O) control dynamically assigns each input pin to a selected one of a plurality of I/O controllers to thereby associate with a selected I/O controller each input pin corresponding to an assignment request. (Spec. 55, l. 18-Spec. 59, l. 12.)

Illustrative Claim

Independent claim 8 further illustrates the invention. It reads as follows:

> 8. A method for dynamically assigning interface pins, said method comprising:
>
> receiving a first assignment request;
>
> identifying one or more interface pins that correspond to the first assignment request;
>
> selecting a first interface controller from a plurality of interface controllers that correspond to the first assignment request; and
>
> associating the identified interface pins with the selected interface controller.

Prior Art Relied Upon

Miller	4,292,668	Sept. 29, 1981
Matsushita	US 6,366,109 B1	Apr. 2, 2002

Rejection on Appeal

Claims 8-27 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over the combination of Matsushita and Miller.

Appellants' Contentions

First, Appellants contend that the combination of Matsushita and Miller does not teach or suggest associating identified pins corresponding to an assignment request with a selected one of a plurality of interface controllers, as recited in independent claim 8. (App. Br. 6-13.) According to Appellants, Matsushita's disclosure of assigning logical semiconductor pins to different physical pins to facilitate the testing of different types of semiconductor packages does not teach selecting an interface controller from a plurality of interface controllers. Likely, Appellants argue that while Miller discloses a plurality of interface controllers, it does not teach selecting a controller based on an assignment request. (App. Br. 9.) Further, Appellants argue that the cited references are directed to different technologies, and that there is insufficient motivation to combine them. That is, Matsushita is directed to semiconductor testing, whereas Miller is an "ancient" reference directed to blocks of data assigned to a particular type of interface controller. (*Id.* at 10-13.)

Examiner's Findings

In response, the Examiner submits that Appellants have opted to improperly attack Matsushita and Miller individually, and not as the combination proffered in the rejection. (Ans. 7-11.) In particular, the Examiner finds that Miller's teaching of selecting an interface controller complements Matsushita's teaching of a data processing system having included therein an interface controller to predictably result in assigning interface requests to controllers as claimed. (*Id.* at 10-15.) Therefore, the Examiner concludes that the cited references are properly combined to render claim 1 unpatentable. (*Id.*)

Therefore, the pivotal issue before us is as follows:

II. ISSUE

Have Appellants shown that the Examiner erred in finding that disclosures of Matsushita and Miller are properly combined to teach or suggest assigning a selected one of a plurality of interface controllers to an identified interface pin corresponding to an assignment request as recited in independent claim 8?

III. FINDINGS OF FACT

The following Findings of Fact (FF) are shown by a preponderance of the evidence.

Matsushita

1. Matsushita discloses a semiconductor testing system having a tester controller that generates a test signal, which it applies to the logical pins of the semiconductor device to thereby convert them into corresponding physical pins according to available pin assignment data. (Col. 2, ll. 40-55.) In particular, the tester controller utilizes a pin assignment convertor containing a map memory that stores pin assignment data, such as address of pins. (Col. 2, ll. 56-67.)

Miller

2. Miller discloses a data processing system having a plurality of I/O processors, each being dedicated to the selection of an I/O device associated therewith. (Fig. 2, abstract.)

IV. ANALYSIS

On the record before us, we find error in the Examiner's rejection of independent claim 8, which recites, *inter alia,* associating identified interface pins with an interface controller selected from a plurality of interface controllers corresponding to a first assignment request. In particular, we do not agree with the Examiner that, at the time of the instant invention, one of ordinary skill in the art would have found sufficient motivation to incorporate Miller's teaching of selecting one of a plurality of dedicated I/O controllers (FF. 2) into Matsushita's semiconductor testing unit (FF. 1) to somehow associate the semiconductor's pins with the selected I/O controller.

First, we agree with the Examiner that Matsushita's testing unit includes a single test controller for testing all the semiconductor's pins, including those assigned with particular requests. (FF. 1.) Further, we agree with the Examiner that Miller's disclosure teaches, upon selecting one of a plurality of I/O devices, a CPU also selects an associated one of a plurality of I/O controllers associated therewith to assist the selected device with a particular task. (FF. 2.) However, we agree with Appellants that Miller's data processing system with data multiplex control bus is far afield from Matsushita's semiconductor testing system. While the cited references do disclose prior art elements that perform their ordinary functions, we fail to find, on this record, any rational underpinning that would have motivated the ordinarily skilled artisan to incorporate Miller's dedicated I/O controllers into Matsushita's testing system to predictably result in a selected controller being associated with an identified pin assigned to a request. We therefore agree that the proffered combination of Matsushita and Miller is a result of impermissible hindsight.

Since Appellants have shown at least one error in the Examiner's rejection, we need not address Appellants' other arguments. It follows that Appellants have shown error in the Examiner's rejection of claim 8.

Because claims 9-27 also recite the limitations of claim 1 discussed above, we find that Appellants have also shown error in the Examiner's rejection of those claims.

V. DECISION

We reverse the Examiner's rejections of claims 8-27 as set forth above.

REVERSED

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